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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,049	09/04/2003	Patrick Lampin	FR920020057	2048
32074 7590 04/03/2007 INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			EXAMINER SU, BENJAMIN	
			ART UNIT	PAPER NUMBER
			2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.		Applicant(s)	
	10/605,049		LAMPIN ET AL.	
	Examiner		Art Unit	
	Benjamin Su		2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

NOTE

1. In claim 1, line 2, the term "adopted to " is not a positively recited claim limitation. Therefore, the limitations after the term are not considered as claim limitations. It is suggested the applicant remove the term. See MPEP 2111.04.
2. Acknowledge is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because it is not on a single sheet and has more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claim 1 is objected to because of the following informalities: For claim 1, line 23, the phrase "the value of the status bits in said second data storage" should be changed to "the value of the status bits into said second data storage". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For claim 1, lines 3 – 4, the term "the dynamic time division multiplexing access method" has no antecedent basis.

For claim 1, line 8, the term "(...,x,...)" is vague and indefinite, it is not known the metes and bounds of the claim.

For claim 1, line 11, the term "the improvement" has no antecedent basis.

For claim 1, line 3, the term "n-bit frames" is indefinite, it is not known the metes and bounds of the claim.

For claim 1, line 10, the term "p bits" is indefinite, it is now known the metes and bounds of the claim.

For claim 1, line 11, the term "the improvement" is vague and indefinite, it is unclear what the improvement improves upon.

For claim 1, line 13, the term "the time slot assignment table" has no antecedent basis.

Claim Rejections - 35 USC § 103

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2616

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Nguyen et al. (US 7042895).

The admitted prior art disclose, regarding claim 1, in a telecommunication system split into a plurality of subsystems adapted to exchange serial data bits arranged in n-bit frames according to the dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position (Bit1 to Bitn) of the frame is associated either one among N logical channels or a null value, N being the maximum number of logical channels (... , X, ...) that can be simultaneously opened and wherein to each logical channel (X) is associated an identifier (LC X) coded on p bits, the improvement comprising:

first data storage means comprising an nxp memory block to store the time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots (TimeslotX, ...) (see paragraph 4, lines 9 – 16);

input bus means for inputting the logical channel identifiers into the first data storage means from a computer or an application software (see paragraph 7, lines 7 – 8);

logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers to an output bus means for subsequent processing by a time slot assignor (see paragraph 6, lines 15 –

20, wherein memory blocks 21-1 and 21-2 correspond to first and second data storage means respectively, multiplexer corresponds to logic circuit means);

The admitted prior art fail to teach second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value;

Nguyen et al. from the same or similar field of endeavors teach second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value (see column 4, lines 50 – 52, 63 – 67, column 5, lines 1 – 3, 48 - 55);

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use second data storage means comprising a Nxl register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value in the method system taught by the admitted prior art in order to allow better system performance by reducing the demand on processor (see column 5, lines 21 – 23).

The admitted prior art fail to teach input bus means for inputting the value of the status bits in the second data storage means from a computer.

Nguyen et al. from the same or similar field of endeavors teach input bus means for inputting the value of the status bits in the second data storage means from a computer (see column 5, lines 22 – 35).

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Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use input bus means for inputting the value of the status bits in the second data storage means from a computer in order to allow accurate channel status record keeping (see column 5, lines 23 – 25).

The admitted prior art fail to teach logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned".

Nguyen et al. from the same or similar field of endeavors teach logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" (see column 6, lines 45 – 55, wherein the tri-state buffer corresponds to logic circuit means).

Thus, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use logic circuit means connected to the first and second data storage means that enables or disables the transmission of the logical channel identifiers depending upon they are "assigned" or "unassigned" in the system taught by the admitted prior art in order to allow efficient bus access control by using only one shift register and storage register (see column 6, lines 50 – 53).

Regarding claim 2, the admitted prior disclose the null value corresponds to a bit position to which none logical channel is assigned (see paragraph 6, lines 6 – 8).

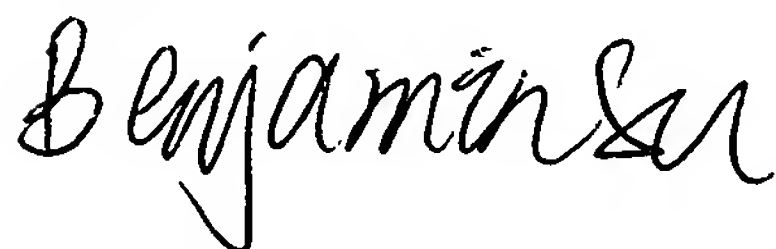
12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chiu et al. (US 6327259) and Nguyen et al. (US 6895016) are cited to show systems which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin Su whose telephone number is 571-270-1423. The examiner can normally be reached on Monday - Friday 10 - 3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BZS



RICKY Q. NGO
SUPERVISORY PATENT EXAMINER